

ABSTRACT

[Para 134] To achieve, by a simple circuit configuration, a DRAM that permits refresh current to be effectively reduced by selectively setting refresh cycles. A memory cell array is divided into 64 subarrays, and each subarray is further divided into 8 blocks. A refresh cycle control circuit has a fuse circuit for setting a frequency dividing ratio of 1 or 1/2, a frequency divider that divides the frequency of a predecode signal by the set frequency dividing ratio, fuse circuits for setting a frequency dividing ratio of 1 or 1/4, and frequency dividers for dividing predecode signals by the set frequency dividing ratio. The refresh cycle control circuit is capable of setting a 64-ms or 128-ms refresh cycle for the 64 subarrays and a 64-ms or 256-ms refresh cycle for 512 blocks.

DRAWINGS